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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,289	09/22/2003	Robert J. Devins	21806-00056-US1	5629

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EXAMINER	
HSU, JONI	
ART UNIT	**PAPER NUMBER**
2671	

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)	
	10/665,289	DEVINS ET AL.	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 29-37 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 29-37 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/5/04, 9/22/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on March 5, 2004 and September 22, 2003 were filed after the mailing date of the application on September 22, 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 29-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peaslee (US005276798A) in view of Dye (US005706478A).

5. With regard to Claim 29, Peaslee describes that the subsystem processor (28, Figure 2) performs the interrupt processing for the host processor (14, Figure 1) (*display list processor 28 comprises an interrupt handler address generator 97, display list command interpreter 93 is coupled to the host processor 14 by way of interrupt lines*, Col. 6, lines 9-31), and therefore discloses a method for offloading hardware interrupt processing from a host system to a subsystem. The method comprises capturing, in a memory (26), as an executable program, hardware instructions generated by high-level specifications of operations in a computer program (*display memory 26 stores all commands, Col. 3, lines 67-68; graphic commands are from host processor 14*, Col. 3, lines 47-50); utilizing a subsystem processor (28) to issue the captured instructions from the memory to subsystem hardware (34, 30) (*display memory 26 is accessible by the display list processor 28*, Col. 4, lines 5-8, *display list processor 28 handles the various ways that commands can be sent to the cogenerator 10*, Col. 5, lines 58-60, *graphics generator 34 is connected to the readback multiplexer 44 for various cogenerator 10 drawing operations, block texturing and complex clipping processor 30 also sends data to the readback multiplexer 44 for various cogenerator 10 operations*, Col. 7, lines 38-43). There is a status indicator (42) containing status information relating to a plurality of operations being carried out on the subsystem hardware (*context registers 42 store all of the cogenerator attributes, these attributes define the current state of the cogenerator 10*, Col. 6, lines 43-45), wherein the subsystem

processor monitors the status indicator and issues the captured instructions in response to the status information (Col. 7, lines 13-27).

However, Peaslee does not teach that the status indicator is included in the subsystem hardware. However, Dye describes a plurality of registers (205, Figure 2) within the subsystem hardware (100) (Col. 7, lines 21-27). These registers contain status indicators (Col. 18, lines 14-18). Therefore, the status indicator is included in the subsystem hardware.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Peaslee so that the status indicator is included in the subsystem hardware as suggested by Dye because Dye suggest that the subsystem hardware can change the status of the operations itself, therefore increasing the processing speed (Col. 21, lines 5-26).

6. With regard to Claim 30, Peaslee describes the captured programs include an instruction for causing the subsystem processor (28, Figure 2) to input an interrupt (Col. 6, lines 9-10, 32-42), and therefore delays issuing instructions in the captured programs.

However, Peaslee does not specifically teach that the interrupt involves delaying issuing instructions in the captured programs until the status indicator contains specified status information. However, Dye describes that the interrupt involves delaying issuing instructions in the captured programs until the status indicator contains specified status information (Col. 16, line 66-Col. 17, line 9).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Peaslee so that the interrupt involves delaying issuing instructions in the captured programs until the status indicator contains specified status

information as suggested by Dye because Dye suggests that this is needed so that the graphics processor (100) knows when to switch out of the idle mode (Col. 16, line 66-Col. 17, line 9).

7. With regard to Claim 31, Peaslee does not teach that the specified status information relates to the completion of a specified operation. However, Dye describes that the specified status information relates to the completion of a specified operation (Col. 20, lines 41-47).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Peaslee so that the specified status information relates to the completion of a specified operation as suggested by Dye because Dye suggests that the graphics processor (100) is only ready to receive more data and instructions after it has completed the current series of instructions (Col. 20, lines 41-47).

8. With regard to Claim 32, Peaslee describes that the subsystem hardware continually performs comparisons between the current bit mapped memory 22 address and the x, y pixel addresses defined by the clipping window boundary (Col. 9, lines 14-18), and therefore repeats the comparison operation periodically, and therefore the operation is repeated periodically.

9. With regard to Claim 33, Peaslee describes that the operation is one of a plurality of operations which are performed serially (*cogenerator attributes are sequentially loaded into the display memory 26*, Col. 7, lines 5-9, Col. 7, lines 16-19, Col. 13, lines 19-23).

10. With regard to Claim 34, Peaslee describes a computer system suitable for graphics rendering (Col. 1, lines 54-55), comprising a host system including at least a CPU (14, Figure 1) and inherently includes a system memory, the host system providing hardware instructions generated by high-level graphics operations executed by the host system (Col. 3, lines 47-50); a graphics subsystem (10) operatively coupled to the host system (Col. 3, lines 47-50), wherein the graphics subsystem contains a display list processor (28, Figure 2) operatively connected to a graphics accelerator (34, 30) (*display list processor 28 handles the various ways that commands can be sent to the cogenerator 10*, Col. 5, lines 54-57, *graphics generator 34 is connected to the readback multiplexer 44 for various cogenerator 10 operations, block texturing and complex clipping processor 30 also sends data to the readback multiplexer 44 for various cogenerator 10 operations*, Col. 7, lines 38-44). There are a plurality of status registers (42; *context registers 42 store all of the cogenerator attributes, these attributes define the current state of the cogenerator 10, current state may include a large number of parameters such as draw pointer position, foreground color, background color, clipping window dimensions, etc.*, Col. 6, lines 43-49) which each indicate a status of a different one of a plurality of graphics operations (*context registers 42 are comprised of 21 attribute registers 101-1 to 101-21*, Col. 6, lines 55-58), wherein the graphics subsystem receives the hardware instructions provided by the host system (Col. 3, lines 47-50). The display list processor performs the interrupt processing for the CPU (*display list processor 28 comprises an interrupt handler address generator 97, display list command interpreter 93 is coupled to the host processor 14 by way of interrupt lines*, Col. 6, lines 9-31), and therefore reduces a requirement for hardware interrupt generation and handling by the CPU.

However, Peaslee does not teach that the plurality of status registers are included in the subsystem hardware. However, Dye describes that the plurality of status registers (205, Figure 2) are included in the subsystem hardware (100, Col. 18, lines 14-18). This would be obvious for the same reasons given in the rejection for Claim 29.

11. With regard to Claim 35, Peaslee describes that at least one of the plurality of graphics operations are operations carried out by the graphics accelerator (34, 30, Figure 2) (*graphics generator 34 is connected to the readback multiplexer 44 for various cogenerator 10 operations, block texturing and complex clipping processor 30 also sends data to the readback multiplexer 44 for various cogenerator 10 operations*, Col. 7, lines 38-44).

12. With regard to Claim 36, Peaslee describes that at least one of the plurality of graphics operations are operations carried out by a hardware device (14, 16, 17, Figure 1) external to the graphics accelerator (34, 30) (Col. 3, lines 25-32).

13. With regard to Claim 37, Claim 37 is similar in scope to Claim 33, and therefore is rejected under the same rationale.

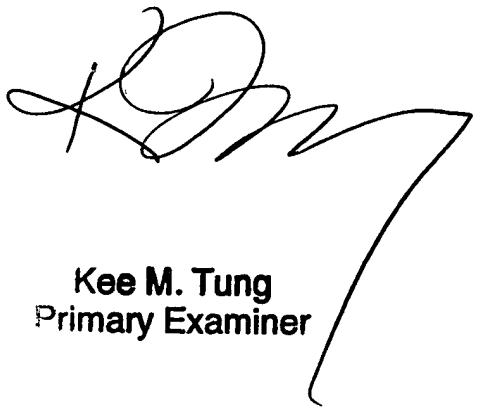
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH



Kee M. Tung
Primary Examiner